

PL4



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/519,187	03/06/2000	William H. Zinger	1424-8124	8441

7590 11/06/2003

Carla Magda Krivak Office of Patent Counsel  
The Johns Hopkins Univ Applied Physics Laboratory  
11100 Johns Hopkins Road  
Laurel, MD 20723-6099

EXAMINER
----------

ZIA, MOSSADEQ

ART UNIT	PAPER NUMBER
----------	--------------

2134

2

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary

Application N .

09/519,187

Applicant(s)

ZINGER ET AL.

Examiner

Mossadeq Zia

Art Unit

2134

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 9 is objected to because of the following informalities: bus is spelled incorrectly. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as anticipated by Patent No. 4,817,140, Chandra et al with additional reference support from Patent No. 5,117,457 Comerford et al. See column 5, line 24-26: both documents describe features of the same embodiment. In regards to Chandra's Figure 1, element 15 should reference coprocessor system 15 (Chandra, col. 17. line 59), and not to disk controller 15.

4. Regarding claim 1, Chandra et al. and Comerford et al. discloses a tamper resistant processor system, comprising:

a multi component chip module (MCM) including:

a CPU (Chandra, fig. 1, element 4);

one or more memory chips (Chandra, fig. 1, element 6, 8); and

one or more chip means containing at least one each of a de-encryption key and algorithm therein (Chandra, fig. 1, element 15, col. 3, line 61-63); and

Art Unit: 2134

an obscurant covering the contents of said multi component chip module

(Chandra, fig. 1, element 155, col. 5, line; Comerford, col. 2, line 47-48);

5. Regarding claim 2, Chandra et al. and Comerford et al. disclose a tamper resistant processor system according to claim 1, further comprising

said multi component chip module in a bus configuration with other multi component (Chandra, fig. 1, element 10, 15, 154, 19 (I/O ports))

chip modules and said one or more memory chips (Chandra, fig. 1, element 6, 8, 151, 152).

6. Regarding claim 3, Chandra et al. and Comerford et al. disclose a tamper resistant processor, system, comprising:

processor boards (Chandra, fig. 1, element 10);

an encrypted computer program (Chandra, col. 3, line 60);

a non volatile memory, operatively connected to said processor boards, for storing

said encrypted computer program (Chandra, fig. 1, element 153, col. 4, line 11-12, col. 6, line 37-39) and sending said encrypted computer programs to address destinations on said processor boards (Chandra, col. 6, line 2-3, 6);

multi-component chip modules (Chandra, fig. 1, element 10, 15, connected by elements 19 and 154) for receiving and de-encrypting said encrypted computer program and sending said de-encrypted computer programs to memory components on said multi component chip modules (Chandra, col. 3, line 60-61, col. 6, line 2-4).

7. Regarding claim 4, Chandra et al. and Comerford et al. disclose a method for protecting a processor system from tampering, said method comprising the steps of:

a) mounting IC components on a single substrate as a multi-component module or as the contents of a multi component module (Chandra, fig. 1, element 4, 10, 15, 150);

b) converting an encrypted computer program, received over a bus from a non-volatile memory, into its original un-encrypted form (Chandra, fig. 1, element 153, col. 4, line 11-12, col. 6, line 37-39);

c) sending the de-encrypted computer program to appropriate locations in memory located in the multi-component module (Chandra, col. 6, line 2-3, 6); and

d) protecting the multi-component module using one or a combination of an obscurant, deceptive patterns, and tamper detection/destruction mechanisms (Comerford, col. 2, line 47-48, 65-67).

8. Regarding claim 5 and 7, see the reasoning for claim 2.

9. Regarding claim 6 and 8, see the reasoning for claim 4.

10. Regarding claim 9, Chandra et al. and Comerford et al. a tamper resistant processor system, comprising:

a multi component chip module including:

a CPU (Chandra, fig. 1, element 4); and

an in-line real time de-encryption chip (Chandra, fig. 1, element 150, col. 17, line 65-66);

one or more memory chips, operatively connected to said in line real time de-encryption chip, said multi-component chip module encrypting out put to said one or more memory chips (Chandra, fig. 1, element 4, 150, col. 16, line 48-50; col. 17, line 65-66); and

Art Unit: 2134

a memory controller selecting between secured and un-secured memory over a processor bus (Chandra, fig. 1, element 10, 15, col. 16, line 51-52).

***Conclusion***


11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mossadeq Zia whose telephone number is 703-305-8425. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Greg Morse can be reached on 703-308-4789. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-3900.

Mossadeq Zia  
Examiner  
Art Unit 2134

Mz  
10/31/03

  
GREGORY MORSE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100